

**WHAT IS CLAIMED IS:**

- 1 1. A circuit arrangement for generating test-traffic on a digital data path having at  
2 least one other traffic source, comprising:  
3 a data-generation circuit adapted to provide a first data stream;  
4 a memory arrangement adapted to buffer a plurality of programmable  
5 commands, the programmable commands indicative of at least one of test-traffic type,  
6 pattern and behavior-in-time;  
7 state machine circuitry coupled between the memory arrangement, the data-  
8 generation circuit and the digital data path, the state machine circuitry adapted to  
9 assemble portions of the first data stream into test-traffic wherein at least one of type,  
10 pattern and behavior-in-time is selected responsive to the programmable commands,  
11 and further adapted to generate test-traffic on the digital data path; and  
12 a status and feedback circuit adapted to monitor the digital data path for test-  
13 traffic and generate a feedback signal indicative of at least one of test-traffic throughput  
14 and test-traffic quality.
- 1 2. The circuit arrangement of claim 1, wherein  
2 the state machine circuitry includes a command state machine and a bus master  
3 state machine, the command state machine being coupled to the memory arrangement  
4 and data-generation circuit, and adapted to direct the bus master state machine to  
5 assemble portions of the first data stream into test-traffic having pre-defined type,  
6 pattern and behavior-in-time responsive to the programmable commands, and  
7 the bus master state machine is coupled to the digital data path and adapted to  
8 communicate the test-traffic onto the digital data path responsive to the command state  
9 machine.
- 1 3. The circuit arrangement of claim 1, wherein the state machine circuitry is  
2 adapted to assemble portions of the first data stream into a test-traffic type selected from  
3 a group consisting of 1, 2, 4, 8, 16, 32, and 64 words per burst.

- 1 4. The circuit arrangement of claim 1, wherein the state machine circuitry is  
2 adapted to assemble portions of the first data stream into a test-traffic type selected from  
3 a group consisting of other than 1, 2, 4, 8, 16, 32, and 64 transfers per burst.
- 1 5. The circuit arrangement of claim 1, wherein the state machine circuitry is further  
2 adapted to receive the first data stream from the data-generation circuit without  
3 generating test-traffic on the digital data path.
- 1 6. The circuit arrangement of claim 1, wherein the state machine circuitry is  
2 adapted to pause in response to programmable commands.
- 1 7. The circuit arrangement of claim 1, further comprising a bus interface circuit  
2 coupled between the memory arrangement and the digital data path, the bus interface  
3 circuit adapted to pass programmable commands received via the digital data path to the  
4 memory arrangement.
- 1 8. The circuit arrangement of claim 1, wherein the first data stream is a repeatable  
2 sequence of binary data.
- 1 9. The circuit arrangement of claim 8, wherein the data-generation circuit is a  
2 second memory arrangement, the first data stream being stored in the second memory  
3 arrangement.
- 1 10. The circuit arrangement of claim 8, wherein the first data stream comprises a  
2 sequence of pseudo-random numbers.
- 1 11. The circuit arrangement of claim 10, wherein the data-generation circuit is a  
2 second memory arrangement, the first data stream being stored in the second memory  
3 arrangement.

1 12. The circuit arrangement of claim 10, wherein the data-generation circuit is a  
2 linear feedback shift register (LFSR) circuit, the first data stream comprising a sequence  
3 of LFSR values.

1 13. The circuit arrangement of claim 12, wherein the state machine circuitry is  
2 configured and arranged to seed the LFSR and control content of the first data stream.

1 14. The circuit arrangement of claim 13, wherein the status and feedback circuit is  
2 further adapted to verify monitored test-traffic against corresponding LFSR values, and  
3 the feedback signal being an interrupt generated indicative of the test-traffic  
4 verification.

1 15. The circuit arrangement of claim 1, wherein the status and feedback circuit is  
2 further adapted to verify monitored test-traffic against a corresponding first data stream,  
3 and the feedback signal being an interrupt generated indicative of the test-traffic  
4 verification.

1 16. The circuit arrangement of claim 15, wherein the memory arrangement includes  
2 command registers adapted to store programmable commands, configuration registers  
3 adapted to store traffic generation process control information and status registers  
4 adapted to store test-traffic verification information.

1 17. The circuit arrangement of claim 1, wherein the status and feedback circuit  
2 includes a counter adapted to specify a number of command repetitions, and a loop  
3 timer adapted to specify a period within which a set of programmable commands must  
4 execute.

1 18. The circuit arrangement of claim 1, wherein the digital data path is an AHB  
2 protocol bus.

1 19. A computer system, comprising:  
2 a digital data path;  
3 a plurality of traffic sources, each traffic source coupled to the digital data path  
4 and adapted to communicate non-test-traffic onto the digital data path; and  
5 a circuit arrangement for generating test-traffic coupled to the digital data path,  
6 the circuit arrangement including,  
7 a data-generation circuit adapted to provide a first data stream,  
8 a memory arrangement adapted to buffer a plurality of programmable  
9 commands, the programmable commands indicative of at least one of test-traffic  
10 type, pattern and behavior;  
11 state machine circuitry coupled between the memory arrangement, the  
12 data-generation circuit and the digital data path, the state machine circuitry  
13 adapted to assemble portions of the first data stream into test-traffic wherein at  
14 least one of type, pattern and behavior-in-time is selected responsive to the  
15 programmable commands, and further adapted to generate test-traffic on the  
16 digital data path; and  
17 a status and feedback circuit adapted to monitor the digital data path for test-traffic and  
18 generate a feedback signal indicative of at least one of test-traffic throughput and test-  
19 traffic quality, wherein at least one of the plurality of traffic sources is a processor  
20 circuit.

1 20. The circuit arrangement of claim 19, wherein the data-generation circuit is a  
2 linear feedback shift register (LFSR) circuit, the first data stream consists of a sequence  
3 of pseudo-randomly generated binary numbers representing LFSR values.

1 21. The circuit arrangement of claim 20, wherein the status and feedback circuit is  
2 further adapted to verify monitored test-traffic against a corresponding first data stream,  
3 and the feedback signal is an interrupt generated indicative of the test-traffic  
4 verification.

1 22. A method of generating test-traffic on a digital data path having at least one  
2 other traffic source, comprising:  
3 coupling a dedicated test-traffic source to the digital data path;  
4 providing a first data stream, the first data stream being replicatable;  
5 storing a plurality of programmable commands, the programmable commands  
6 indicative of at least one of test-traffic type, pattern and behavior;  
7 assembling portions of the first data stream into test-traffic wherein at least one  
8 of type, pattern and behavior-in-time is selected responsive to the programmable  
9 commands;  
10 generating test-traffic on the digital data path;  
11 monitoring the digital data path for the test-traffic;  
12 verifying the monitored test-traffic against a corresponding first data stream; and  
13 generating a feedback signal indicative of the test-traffic verification.

1 23. The method of claim 22, wherein the first data stream is a sequence of pseudo-  
2 random numbers each representative of a linear feedback shift register (LFSR) value.

1 24. The method of claim 23, further comprising, verifying monitored test-traffic  
2 against a corresponding LFSR value, wherein the feedback signal is an interrupt  
3 indicative of each test-traffic verification.

1 25. The method of claim 22, further comprising:  
2 counting a pre-determined number of command-execution repetitions;  
3 timing each command-execution repetition against an associated programmable  
4 period; and  
5 generating a feedback signal indicative a command-execution repetition  
6 exceeding the associated programmable period.

1 26. The method of claim 22, wherein the digital data path is an AHB protocol bus.

1 27. The method of claim 26, wherein  
2 test-traffic type is one of a group consisting of 1, 2, 4, 8, 16, 32, and 64 transfers  
3 per burst.

1 28. A circuit arrangement for generating test-traffic on a digital data path having at  
2 least one other traffic source, comprising:  
3 means for coupling a dedicated test-traffic source to the digital data path;  
4 means for providing a first data stream, the first data stream being replicatable;  
5 means for storing a plurality of programmable commands, the programmable  
6 commands indicative of at least one of test-traffic type, pattern and behavior;  
7 means for assembling portions of the first data stream into test-traffic wherein at  
8 least one of type, pattern and behavior-in-time is selected responsive to the  
9 programmable commands;  
10 means for generating test-traffic on the digital data path;  
11 means for monitoring the digital data path for the test-traffic;  
12 means for verifying the monitored test-traffic against a corresponding first data  
13 stream; and  
14 means for generating a feedback signal indicative of the test-traffic verification.

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